DIGITAL SYSTEMS

Exercise Book

Information Representation

1. Convert each number to base 10:
   a)
      i) 1101110.101_2
      ii) 0.00101_2
      iii) 1011010.1010_2
   b)
      i) $1FD.8_{16}$
      ii) $A2C1_{16}$
      iii) $1A.B2_{16}$

2. Convert the decimal number 467.75 to its equivalent format in binary and hexadecimal.

3. Convert each one of the following binary numbers into hexadecimal:
   a) 1111000010.01
   b) 111100101011.110111
   c) 1010101001.011

4. Convert each of the following hexadecimal numbers into binary:
   a) $4B6.3_{16}$
   b) $8F3.B_{16}$
   c) $4D5.65_{16}$

5. Express each of the following decimal numbers as a one byte binary sequence using the sign and modulus, one's complement and two's complement codding:
   a) +55
   b) -45
   c) -114

6. Convert each binary coded number into decimal:
   a) Signal and modulus
      i) 00010101
      ii) 10010111
   b) One's complement 1
      i) 01101011
      ii) 11011100
   c) Two's complement 2

i) 01110111
ii) 11101000
iii) 10000000

Boolean algebra and logical diagrams

7. Build the following logic diagram for each logical expression:

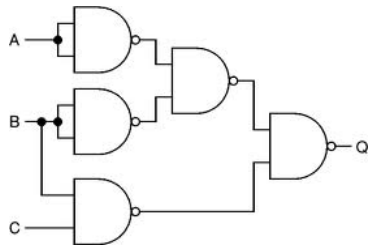
a) $F(x,y,z) = \overline{(\overline{x} \cdot y + z)} + \overline{\overline{x} + z}$

b) $F(x,y,z) = \overline{(x + \overline{y}) \otimes (\overline{x} \cdot z + y)}$

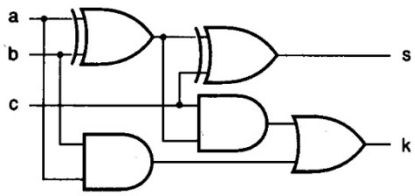
c) $F(x,y,z,w) = \overline{(x \cdot \overline{\overline{(y \cdot z + w)}} + \overline{x} \cdot \overline{y} \cdot z)}$

8. Write the Boolean expression regarding each of the following:

a)



b)



9. Draw the logical diagram of the following Boolean expression:

a) $F(x,y,z,w) = \overline{w \cdot (\overline{x} \cdot y + \overline{y} \cdot z) + \overline{\overline{w \cdot z}}}$

b) $F(x,y,z) = \overline{(\overline{x + \overline{y}}) \oplus (\overline{\overline{x}.y}.z)}$

10. Using the Boolean theorems prove each of the following identities:

a) $x.(x + y) = x$

b) $x + \overline{x}.y = x + y$

c) $(x + \overline{y} + xy).(x + y).\overline{x}.y = 0$

11. Using the Bool's theorems simplify each of the following expressions:

a) $\overline{x}.z + \overline{x}.\overline{z} + x.y$

b) $\overline{x}.\overline{y}.z + x.\overline{y}.z + x.y.z$

c) $\overline{x}.z + \overline{x}.\overline{y}.z + x.y.z$

12. Write the conjunctive and disjunctive Boolean form of each of the following truth tables:

a)

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b)

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

c)

x	y	z	w	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

13. Using a truth table show the following equality:

$$x \oplus y \oplus z = x.y.z + x.\overline{y}.\overline{z} + \overline{x}.y.\overline{z} + \overline{x}.\overline{y}.z$$

14. Rewrite the expression $\overline{y}.(x + \overline{z}) + \overline{x}.y$ in both the disjunctive and conjunctive forms:

a) Using a truth table;

b) Using the theorems of the Boolean algebra.

Aritmética Binária

15. Execute the following operations in base - 2:

a) 101.011 + 11.1101

b) 1111.01 + 10.011

c) 1011.10 - 10.01

d) 111.11 - 10

e) 101 x 100.01

f) 11001.1 x 101.01

Karnaugh Maps

16. Simplify the following expressions using the Karnaugh maps:

a) $F(A,B,C) = \sum(0,1,3)$

b) $F(A,B,C) = \sum(0,1,2,6,7)$

c) $F(A,B,C,D) = \prod(0,2,4,6,8,10,12,14)$

d) $F(A,B,C,D) = \prod(1,2,4,5,7,8,10,11,13,15)$

e) $F(A,B,C,D) = \overline{A}.\overline{B}.C + A.D + B.\overline{D} + C.\overline{D} + A.\overline{C} + \overline{A}.\overline{B}$

f) $F(A,B,C,D) = (A + B + \overline{C}).(\overline{B} + \overline{D}).(\overline{A} + C).(B + C)$

g) $F(A,B,C,D) = \sum(0,1,4,5,9,11,14,15) + X(10,13)$

h) $F(A,B,C,D,E) = \sum(0,3,4,6,11,13,18,19,25,26,31)$

i) $F(A,B,C,D,E) = \sum(1,2,4,6,12,20,22,24,26) + X(0,3,5,11,16,17)$

j) $F(A,B,C,D,E) = A + B.C + \overline{C}.D.\overline{E}$

k) $F(A,B,C,D,E) = (A + B).(B + C).(C + \overline{D}).(D + \overline{E})$

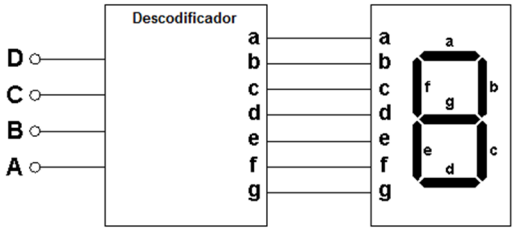
Combinatory Logic Applications

17. Design a digital automation system able to do the following task:

"A water tank is filled by a pump that draws water from a well. The deposit serves for irrigation and water supply to a private house. It is intended that the pump is put into operation only when one takes water for irrigation and house consumption or when the water tank is below a certain level".

Design the circuit by using only NAND gates.

18. Determine the sum of products expression for a BCD to 7 segments decoder, taking advantage of the existence of terms for which the outputs are not defined.



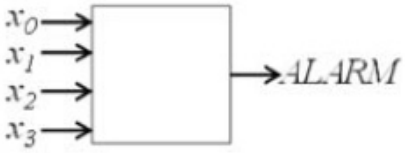
19. Design a digital circuit that receive a 4 bit binary word X coded in BCD and returns a signal M = 1 if X is larger or equal to 7 and M = 0 otherwise. Obtain the logical expression that relates M with X.

20. The patients of an observation room are monitored continuously by an electronic system that generates, at a 5 second interval four signals X0, X1, X2 e X3 with the following information:

- X0 e X1 indicates the actual measured parameter;
- X2 e X3 specify if its value is high, low or acceptable.

The following tables describes each of the signals. The alarm system receive this 4 bits and generate a signal when one or more of the following conditions occur:

- SBP is high
- DBP is low or high
- HR is low or high
- SpO2 is low.



x0	*x1*	Parâmetro
0	0	Pressão arterial sistólica (PAS)
0	1	Pressão arterial diastólica (PAD)
1	0	Frequência cardíaca (FC)
1	1	Saturação de oxigénio (SpO2)

x2	*x3*	Valor Medido
0	0	Baixo
0	1	Aceitável
1	0	Alto
1	1	----

Descodificadores e Multiplexers

21. Design a 4-line decoder by using only NAND gates.

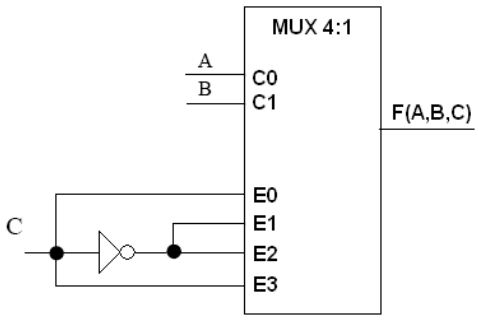
22. Implement the function F using a multiplexer 4-1

x	**y**	**z**	**F**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	1
1	1	1	0

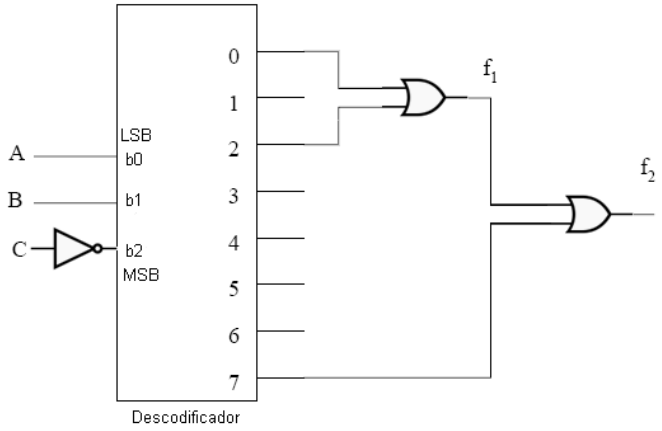
23. Implement the function *F* using a multiplexer 8-1

$$F(X,Y,Z) = \Sigma\,(0, 1, 5)$$

24. Obtain the logic function F(A,B,C) of the following combinatorial circuit built around a 4:1 multiplexer.



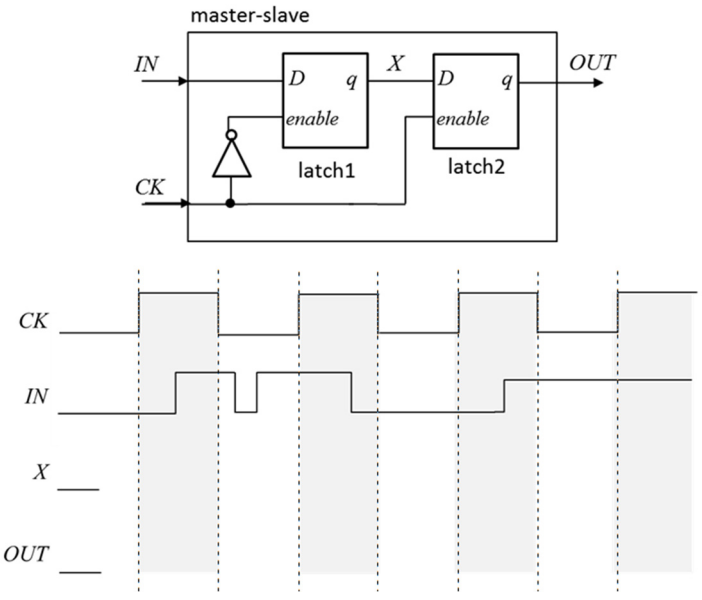
25. Consider the following combinatory circuit built around a 3 to 8 line decoder.



Assuming A=0, B=0 e C=0 obtain the logical value at the output of each of the two OR gates.

Contadores

26. The following circuit has two D latches connected in a mater-slave configuration. Draw the remain waves of the time diagram.



27. Observe the following counter:

Draw the transition table assuming initially Q0=Q1=Q2=Q3=0

28. Design asynchronous counters for the following counting sequence:
    a) 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 0, 1, ...
    b) 8, 9, 10, 11, 12, 13, 14, 8, 9, ...

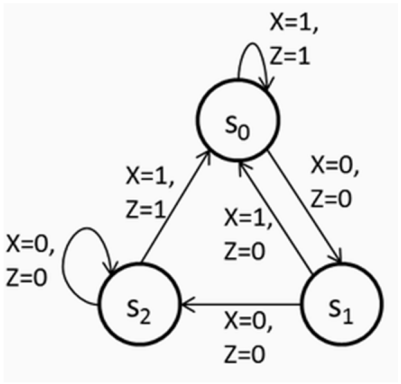
29. Design synchronous counter circuits using JK flip-flop's for the following output sequences:
    a) 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 0, 1, ...
    b) 7, 6, 5, 4, 3, 7, 6, ...

30. Design a synchronous counter using only 3 D flip-flop's for the following counting sequence:

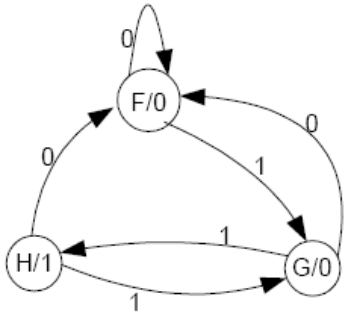
1, 3, 5, 7, 9, 14, 21, 55

Sequential Circuits

31. Draw the state transition table for the following state machine assuming: (a) D type Flip-Flop's and (b) JK Flip-Flop's.

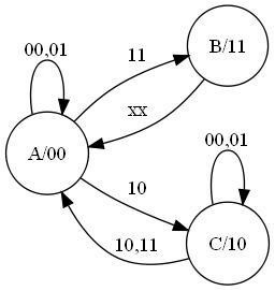


32. The sequential circuit represented by the following state machine diagram has an input E (besides the clock input) and one output S.



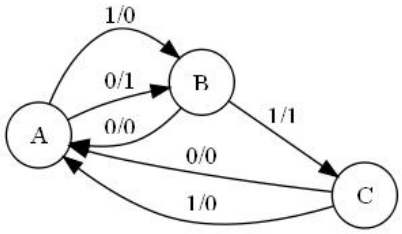
Design the corresponding circuit using D type flip-flop's.

33. The sequential circuit represented by the following state duiagram has two inputs <E0 E1> and two outputs <S0 S1>.



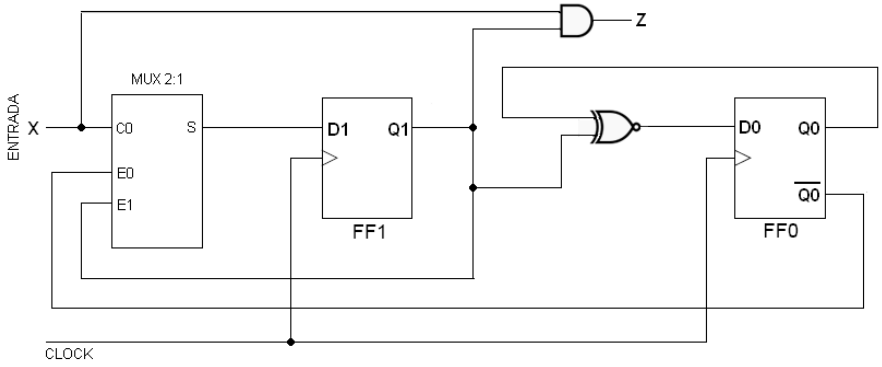
Obtain the transition table assuming JK flip-flop's. Obtain the excitation equations and draw the logical diagram.

34. Observe the following state diagram with an input (X) and one output (Z) and three states (A,B e C):



Obtain the state transition table assuming JK flip-flop's. Obtain the excitation equations and draw the logical diagram.

35. Observe the following circuit with one external input (X) and one output (Z):



Obtain the output logical function at the multiplexer (S) as a function of the variables X, $Q1$ e $\overline{Q0}$.

36. Design a digital circuit for controlling a gate for vehicles access. The circuit receive four inputs::
    - REQUEST: When the driver press a button (REQUEST=1);
    - UP: A sensor installed in the gate with the value 1 when totally open;
    - DOWN: A sensor installed in the gate with the value 1 when totally closed;
    - SENSORS: Return 0 when the gate area is free of vehicles.

    The circuit generate two outputs:
    - ON/OFF: Gate motor off (ON/OFF=0) or on (ON/OFF=1)
    - UP/DOWN: Indicates the gate movement direction (UP/DOWN = 0 opening and UP/DOWN = 1 closing).

    The controller circuit must perform the following operation sequence:
    - Wait for a request (REQUEST=1)
    - Open the gate (ON/OFF=1, UP/DOWN=0)
    - Wait until the gate is totally open (UP=1)
    - Wait for the vehicle area is free (SENSORS=0) and begin closing the gate (ON/OFF=1, UP/DOWN=1)
    - Wait until the gate is completely closed (DOWN=1) and return to the initial state.

    No access request should be considered if the above sequence is not yet finished.

37. Consider a system for detecting the movement of a machine-tool. This movement is detected by a sensor composed by a pair of optical sensors and a ribbon with two different zones.

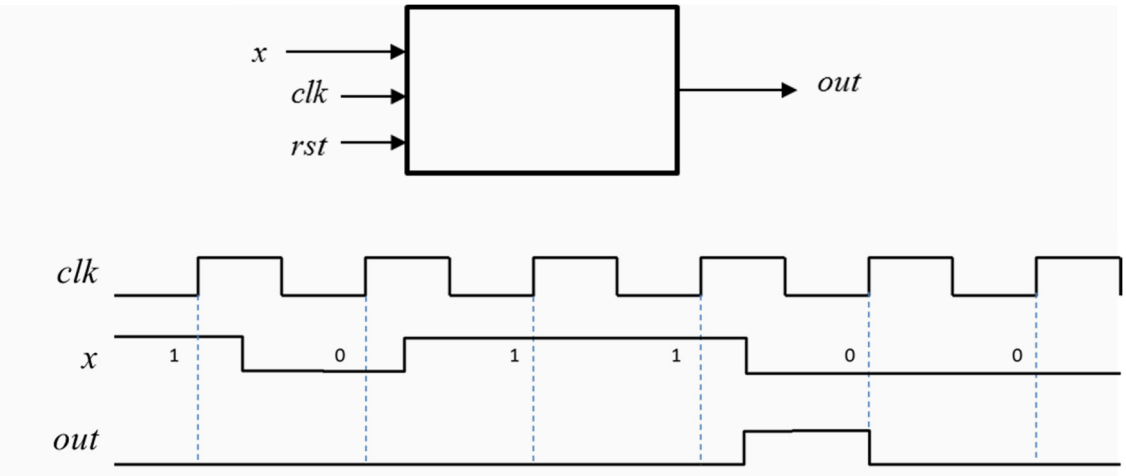
It is intended to design a circuit that drive its output to ‘0’ if the movement of the head is made from the left to right and ‘1’ otherwise.

38. Design a Mealy machine with one input X and one output Y such as the output is '1' when the following sequence is detected:

    - The first bit must be '1',
    - Then at least one zero must follow '0',
    - Then one must observe two '1' and one '0'.

    Once the sequence is detected, the circuit must return to the initial state and wait for a new possible sequence.

    Besides the input X the circuit must possess one clock input and one asynchronous RESET input. The following figure illustrates its input output signals and a possible operating sequence.



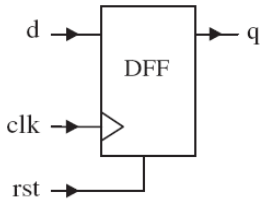
VHDL

39. Build a VHDL library where one can find all the logical operators assuming an arbitrary rise and falling time. This value must be zero by default.

40. Write the entity and architecture for a three input digital circuit that emulates the behaviour of the following truth table:

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

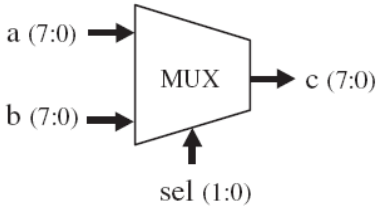
41. The following figure illustrate the diagram of a rising edge D flip-flop with asynchronous input RESET.



Describe its behaviour using VHD.

42. Describe and test the behaviour of an asynchronous RS latch VHDL

43. Describe and simulate the behaviour of a digital switch with two inputs, **a** and **b**, of 8 bit and one output port, **c**, of one byte length. The selection of the input signal to drive the output is controlled by an additional (**sel**) input. The circuit must cope with the truth table presented below:



sel	c
00	0
01	a
10	b
11	1

44. Write a VHDL code to describe the following state machine. Write also a testbench.